

# 54AC16652, 74AC16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCAS242A – MARCH 1990 – REVISED APRIL 1996

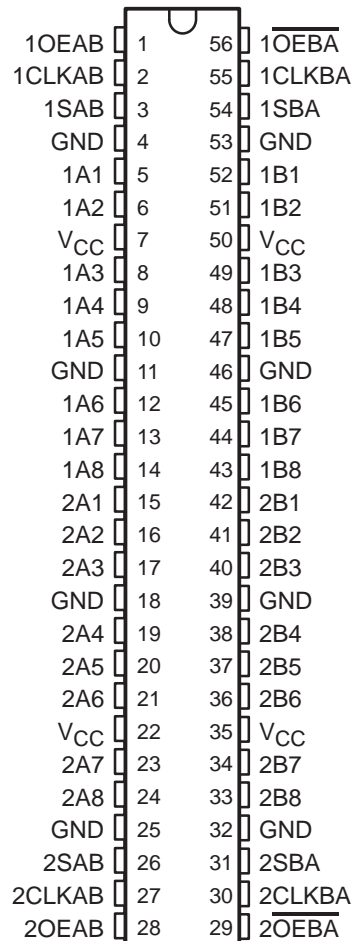
- **Members of the Texas Instruments Widebus™ Family**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

## description

The 'AC16652 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. They can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'AC16652.

54AC16652 . . . WD PACKAGE  
74AC16652 . . . DL PACKAGE  
(TOP VIEW)



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**description (continued)**

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74AC16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16652 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.



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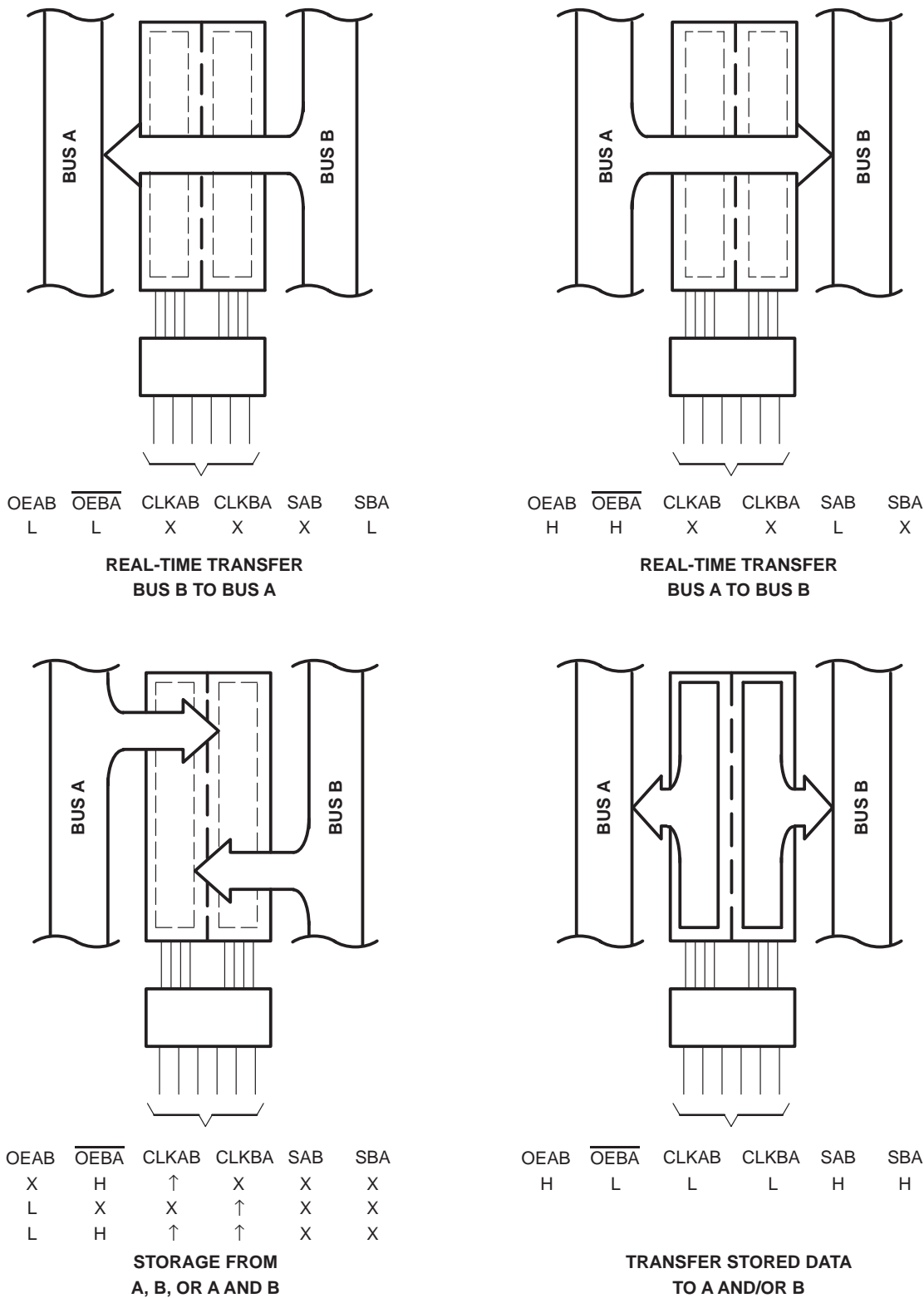
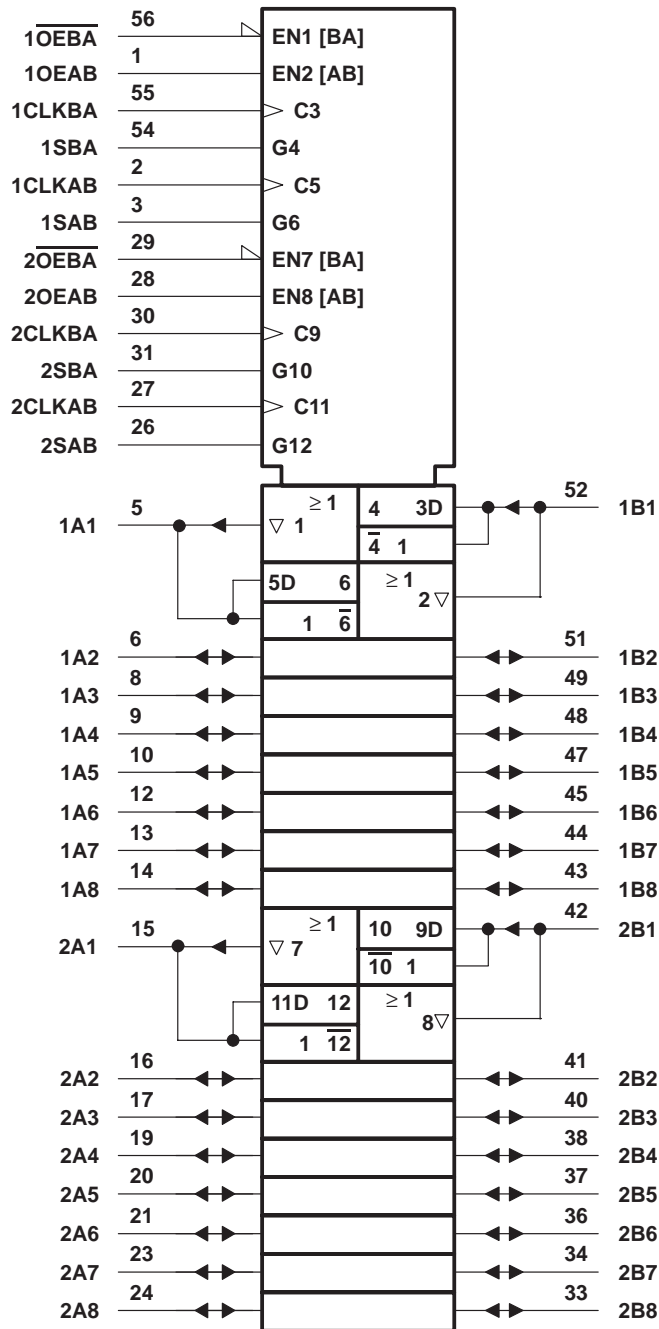


Figure 1. Bus-Management Functions

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## logic symbol†

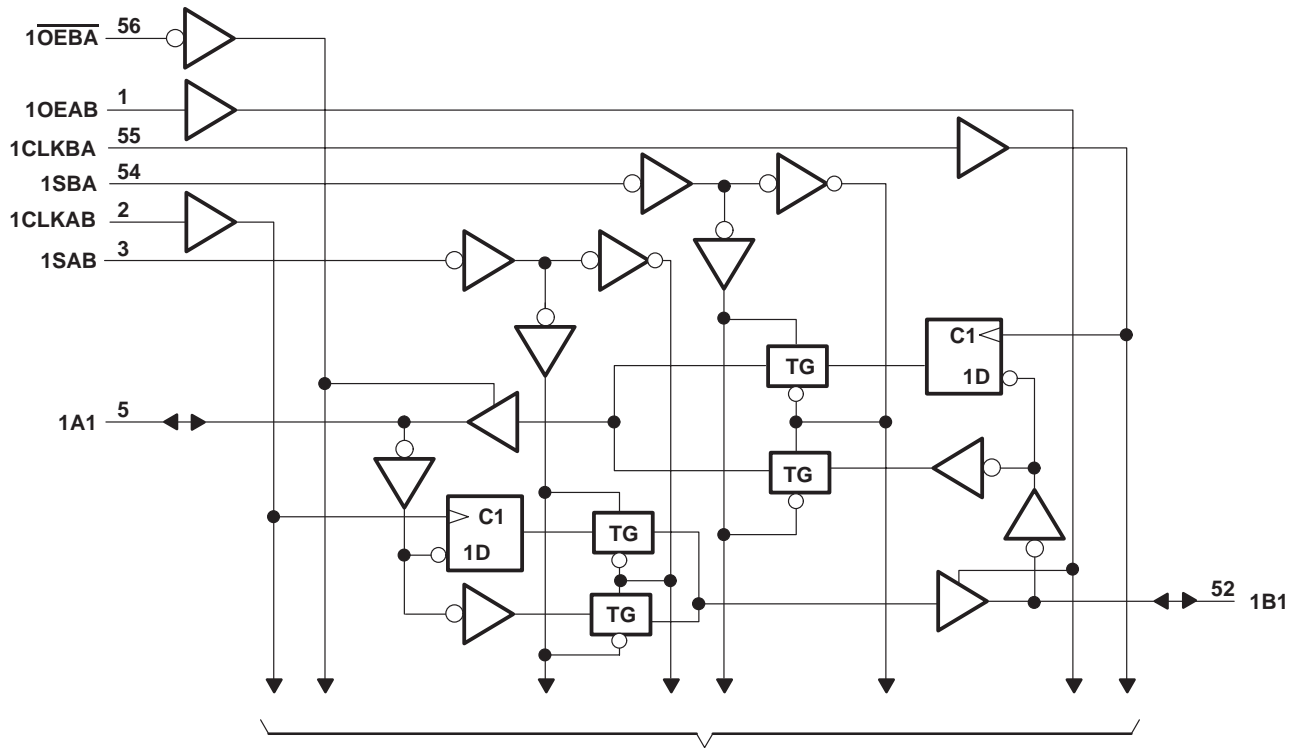


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

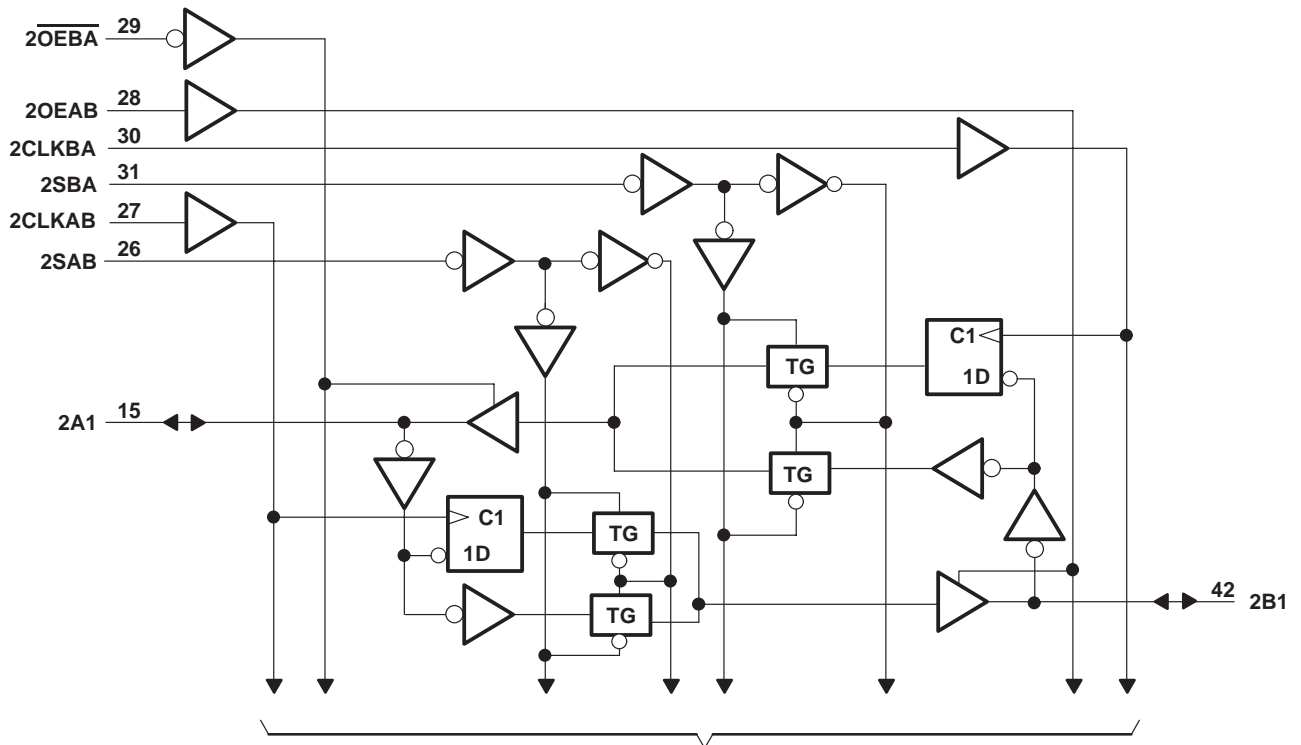
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logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

		54AC16652			74AC16652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage (see Note 4)	3	5	5.5	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V		2.1	2.1		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 5.5$ V		3.85	3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V			0.9		V	
		$V_{CC} = 4.5$ V			1.35			
		$V_{CC} = 5.5$ V			1.65			
$V_I$	Input voltage	0		$V_{CC}$	0	$V_{CC}$	V	
$V_O$	Output voltage	0		$V_{CC}$	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 3$ V			–4		mA	
		$V_{CC} = 4.5$ V			–24			
		$V_{CC} = 5.5$ V			–24			
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V			12		mA	
		$V_{CC} = 4.5$ V			24			
		$V_{CC} = 5.5$ V			24			
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0	10	ns/V	
$T_A$	Operating free-air temperature	–55		125	–40	85	°C	

- NOTES: 3. Unused inputs must be held high or low to prevent them from floating.  
4. All  $V_{CC}$  and GND pins must be connected to the proper voltage power supply.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54AC16652		74AC16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9	2.9		V	
		4.5 V	4.4			4.4	4.4			
		5.5 V	5.4			5.4	5.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.4	2.48			
		4.5 V	3.94			3.7	3.8			
	I <sub>OH</sub> = -24 mA	5.5 V	4.94			4.7	4.8			
		I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V				3.85			
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V					3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1	0.1		V	
		4.5 V				0.1	0.1			
		5.5 V				0.1	0.1			
	I <sub>OL</sub> = 12 mA	3 V				0.36	0.5			
		4.5 V				0.36	0.5			
	I <sub>OL</sub> = 24 mA	5.5 V				0.36	0.5			
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V					1.65		
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V					1.65			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1	±1	μA	
I <sub>OZ</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.5			±10	±5	μA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			160	80	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4					pF	
C <sub>iO</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	12					pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)**

		T <sub>A</sub> = 25°C		54AC16652		74AC16652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	55	0	55	0	55	MHz
t <sub>w</sub>	Pulse duration, CLKAB or CLKBA high or low	9		9		9		ns
t <sub>su</sub>	Setup time, A before CLKAB <sup>↑</sup> or B before CLKBA <sup>↑</sup>	7		7		7		ns
t <sub>h</sub>	Hold time, A after CLKAB <sup>↑</sup> or B after CLKBA <sup>↑</sup>	0		0		0		ns

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)**

		T <sub>A</sub> = 25°C		54AC16652		74AC16652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	95	0	95	0	95	MHz
t <sub>w</sub>	Pulse duration, CLKAB or CLKBA high or low	5		5		5		ns
t <sub>su</sub>	Setup time, A before CLKAB <sup>↑</sup> or B before CLKBA <sup>↑</sup>	4.5		4.5		4.5		ns
t <sub>h</sub>	Hold time, A after CLKAB <sup>↑</sup> or B after CLKBA <sup>↑</sup>	0		0		0		ns

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**54AC16652, 74AC16652**  
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**switching characteristics over recommended operating free-air temperature range,**  
**V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54AC16652		74AC16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			55			55		55		MHz
t <sub>PLH</sub>	A or B	B or A	3.6	10.4	13.7	3.6	17.1	3.6	15.6	ns
t <sub>PHL</sub>			4.1	10.9	14.3	4.1	16.3	4.1	15.4	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	5.1	13.6	17.3	5.1	21.2	5.1	19.5	ns
t <sub>PHL</sub>			5.4	13.5	17.2	5.4	19.9	5.4	18.8	
t <sub>PLH</sub>	SBA or SAB (with A or B high)	A or B	5.8	15.0	18.7	5.8	23.3	5.8	21.4	ns
t <sub>PHL</sub>			5.4	13.1	16.7	5.4	19.1	5.4	18.1	
t <sub>PLH</sub>	SBA or SAB (with A or B low)	A or B	4.2	11.8	15.2	4.2	18.9	4.2	17.4	ns
t <sub>PHL</sub>			5.9	14.4	18.3	5.9	21.7	5.9	20.3	
t <sub>PZH</sub>	$\overline{OEBA}$	A	4.2	11.8	15.1	4.2	18.8	4.2	17.2	ns
t <sub>PZL</sub>			6	16.2	20.6	6	25.3	6	23.5	
t <sub>PHZ</sub>	$\overline{OEBA}$	A	4.6	8.1	10	4.6	10.9	4.6	10.6	ns
t <sub>PLZ</sub>			4.4	7.6	9.6	4.4	10.6	4.4	10.3	
t <sub>PZH</sub>	OEAB	B	4.1	11.5	14.6	4.1	18.1	4.1	16.6	ns
t <sub>PZL</sub>			6	16.0	20	6	24.6	6	22.7	
t <sub>PHZ</sub>	OEAB	B	4.3	7.2	9	4.3	9.7	4.3	9.5	ns
t <sub>PLZ</sub>			3.9	6.7	8.6	3.9	9.2	3.9	9.1	

**switching characteristics over recommended operating free-air temperature range,**  
**V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54AC16652		74AC16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			95			95		95		MHz
t <sub>PLH</sub>	A or B	B or A	2.7	6.1	8.8	2.7	10.7	2.7	9.9	ns
t <sub>PHL</sub>			3	6.3	9.2	3	10.8	3	10.2	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	3.9	7.8	10.9	3.9	13.3	3.9	12.2	ns
t <sub>PHL</sub>			4.2	7.8	11.1	4.2	13.2	4.2	12.3	
t <sub>PLH</sub>	SBA or SAB (with A or B high)	A or B	4.5	8.8	12.1	4.5	15	4.5	13.8	ns
t <sub>PHL</sub>			4.1	7.7	11	4.1	12.9	4.1	12.1	
t <sub>PLH</sub>	SBA or SAB (with A or B low)	A or B	3.1	6.7	9.7	3.1	11.9	3.1	11	ns
t <sub>PHL</sub>			4.6	8.8	12.2	4.6	14.9	4.6	13.8	
t <sub>PZH</sub>	$\overline{OEBA}$	A	3.1	6.7	9.5	3.1	11.6	3.1	10.7	ns
t <sub>PZL</sub>			4.5	8.3	11.8	4.5	14.4	4.5	13.2	
t <sub>PHZ</sub>	$\overline{OEBA}$	A	4.6	6.5	8.3	4.6	9	4.6	8.8	ns
t <sub>PLZ</sub>			4.1	6.1	8.1	4.1	9.1	4.1	8.7	
t <sub>PZH</sub>	OEAB	B	3.1	6.6	9.3	3.1	11.3	3.1	10.5	ns
t <sub>PZL</sub>			4.6	8.2	11.6	4.6	14.1	4.6	13	
t <sub>PHZ</sub>	OEAB	B	4.2	5.9	7.7	4.2	8.3	4.2	8	ns
t <sub>PLZ</sub>			3.7	5.5	7.4	3.7	8.3	3.7	7.8	

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AC16652DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16652DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16652DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16652DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC16652DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC16652DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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